AMENDMENTS TO THE CLAIMS

1-26. (Cancelled)

27. (New) A memory device comprising:

at least one synchronous controlled global element; and

a plurality of self-timed local elements, wherein at least one of said self-timed local elements interfaces with said synchronous controlled global element.

28. (New) The memory device of Claim 27, wherein said at least one synchronously controlled global element includes a global predecoder.

29. (New) The memory device of Claim 27, wherein said at least one synchronously controlled global element comprises at least one global decoder.

30. (New) The memory device of Claim 27, wherein said at least one synchronously controlled global element comprises at least one global controller.

31. (New) The memory device of Claim 27, wherein said at least one synchronously global element comprises at least one global sense amplifier.

32. (New) The memory device of Claim 27, wherein said plurality of self-timed local elements comprises a plurality of memory cells forming at least one cell array.

33. (New) The memory device of Claim 27, wherein said plurality of self-timed local elements comprises at least one local decoder.

34. (New) The memory device of Claim 27, wherein said plurality of self-timed ocal elements comprises at least one local sense amplifier.

35. (New) The memory device of Claim 27, wherein said plurality of self-timed local elements comprises at least one cluster.

36. (New) The memory device of Claim 27, wherein said plurality of self-timed controlled local elements comprises at least one block.

37. (New) The memory device of Claim 27, wherein said block comprises at least one sub-block.

38. (New) The memory device of Claim 27, wherein said plurality of self-timed local elements comprise:

a plurality of memory cells forming at least one cell array;

at least one local decoder interfacing with said at least one cell array;

at least one local sense amplifier interfacing with said local decoder and said cell array and adapted to precharge and equalize at least one line coupled thereto; and

at least one local controller interfacing with and coordinating at least said local decoder and sense amplifier.

39. (New) The memory device of Claim 38, wherein said plurality of self-timed local elements further comprise at least one cluster.

40. (New) The memory device of Claim 27 comprising a plurality of synchronous controlled global elements.

41. (New) The memory device of Claim 40, wherein at least two of said self-timed local elements interface with at least two different synchronous controlled global elements.

42. (New) A synchronous self-timed memory structure comprising:

a plurality of memory cells forming at least one cell array;

at least one self-timed local decoder interfacing with said at least one cell array;

at least one self-timed local sense amplifier interfacing with at least said one self-timed controlled local decoder and said cell array and adapted to precharge and equalize at least one line coupled thereto; and

at least one self-timed local controller interfacing with and coordinating said self-timed local decoder and said self-timed sense amplifier.

43. (New) The memory structure of Claim 42, further including at least one line replicating a global bit line interfacing with said self-timed local controller.

44. (New) The memory structure of Claim 42, wherein said self-timed local sense amplifier is adapted to multiplex at least two sense amplifiers.

45. (New) The memory structure of Claim 42, wherein said self-timed local sense amplifier is adapted to multiplex four sense amplifiers to a multiplexed line coupled to said self-timed local sense amplifier.

46. (New) A synchronous controlled hierarchical memory structure that comprises a logical portion of a larger memory device, the hierarchical memory structure comprising:

a plurality of memory cells forming at least one cell array;

at least one self-timed local decoder interfacing with said at least one cell array;

at least one self-timed local sense amplifier interfacing with said at least one self-timed local decoder and said at least one cell array and adapted to precharge and equalize at least one line coupled thereto; and

at least one self-timed local controller interfacing with and coordinating said at least one self-timed local decoder and said at least one self-timed local sense amplifier.

47. (New) A method of performing a read operation using a synchronously controlled memory device containing at least one logical memory subsystem, the method comprising:

selecting at least one cell array;

selecting at least one sub-block in the logical memory subsystem;

isolating at least one self-timed local sense amplifier;

activating a local wordline;

discharging at least one bitline in at least one bitline pair;

developing a differential voltage across said bitline pair;

stopping said discharge; and

equalizing and precharging said bitline pair.

48. (New) The method of Claim 47, further comprising activating at least one mux line to select said cell array.

49. (New) A method of performing a write operation using a memory device containing at least one logical memory subsystem, the method comprising:

receiving data transmitted on at least one write bank line;

transmitting a high signal on a local word line;

selecting at least one memory cell.

50. (New) The method of Claim 49 further comprising completing the write operation when said local word line is high.

51. (New)The method of Claim 49 wherein a global controller receives said data transmitted on said at least one write bank line.

52. (New) The method of Claim 49 wherein a global sense amp receives said data transmitted on said at least one write bank line.

53. (New) The method of Claim 49 wherein data to be written in said at least one memory cell is put onto a global bit line synchronously with said at least one local write bank line.